

EE457: Digital IC Design

Fall Semester 2015

Project #3 Report Cover Sheet

Due 11/25/2015, 5:00PM in ST-630

## **PROJECT TITLE:**

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Note: Label your figures and tables. Reference them in your text and discuss your results.

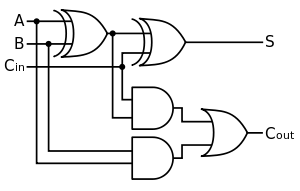
**Executive Summary:**

In this project we will be to create a 6bit adder. We are going to use the same program that we have been using Electric to draw schematics and layouts. We will also be checking our schematics and layouts, using IRSIM and LTSPICE to make sure our project is working as expected. We need to make sure that the adders are all working to par and that they not only add but also subtract. We will be using six 1bit adders in parallel to make the complete six bit adders with carry. To check for correctness we use the DRC in schematics and the well checks in layouts. For the layout we find and implement the correct Euler's path that works correctly with the adders. The layout will have basically six repeats of the adder but with different inputs. We have inputs A0 – A6, B0 – B6, Cin, Cout, and Sum – Sum5. Since we are doing project 3b we will be implementing the carry-look ahead adders. This kind of adder reduces the propagation delay. Finally when all is done we complete DRC and well checks, once that is done we perform simulations on IRSIM and LTSPICE for all inputs and for inputs A0 and B2 we use the pulse function, this should match the logic in the additions and subtraction.

**Introduction:**

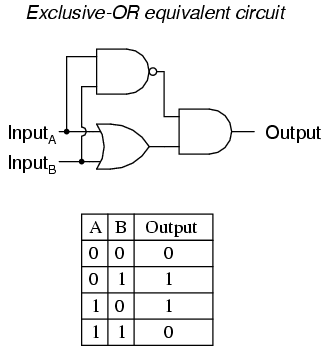
In this project we use adders in parallel to do addition and subtraction. With 1bit full adders it adds three 1bit numbers, we use, *B*, and *C*in; *A* and *B* are the numbers we are adding, and *C*in is a bit carried in. When we cascade then and we can get higher level additions such as our 6bit adder with a ripple carry logic. This can be used at different number of adders to create larger adders. First we have design the schematic of a 1 full bit adder with carry in. For this we must first take a look at the gates in a 1 bit adder.

**Figure 0.1 Schematic of 1 bit adder with carry in (using gates)**



As seen in the figure above we need to the schematic contains two exclusive-or gates and a combination of two and gates and an or gate. We must further break down the exclusive-or gate into NAND, OR and AND gates (as shown below).

**Figure 0.2 Equivalent logical circuit of Exclusive-or Gate**

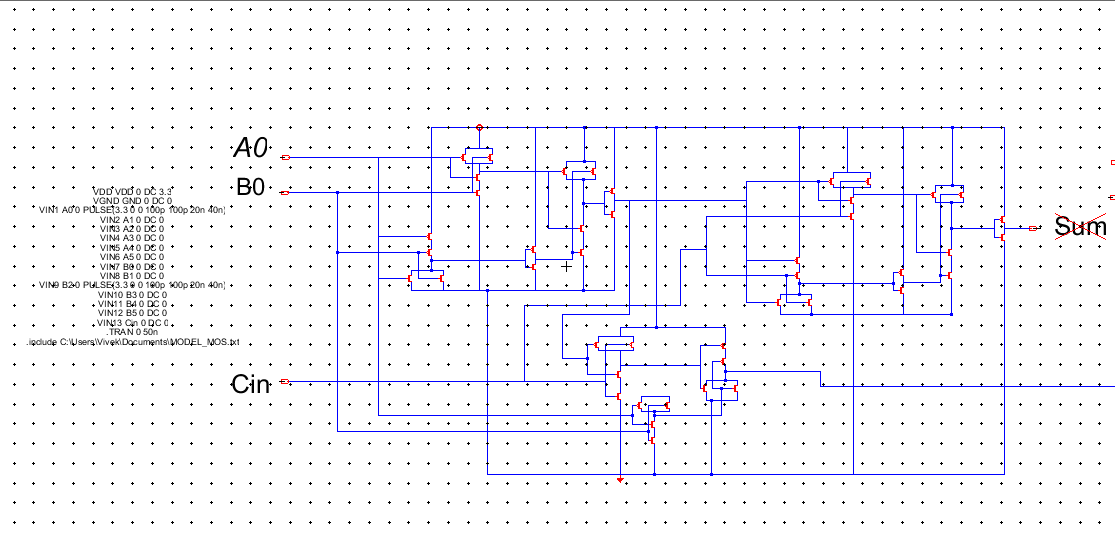


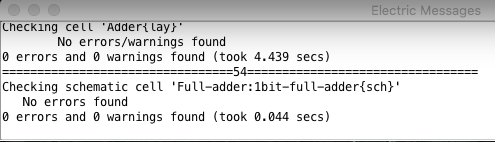
Now that we have simplified all the gates, we can design them using transistors and design the adder.

**Approach and Calculations:**

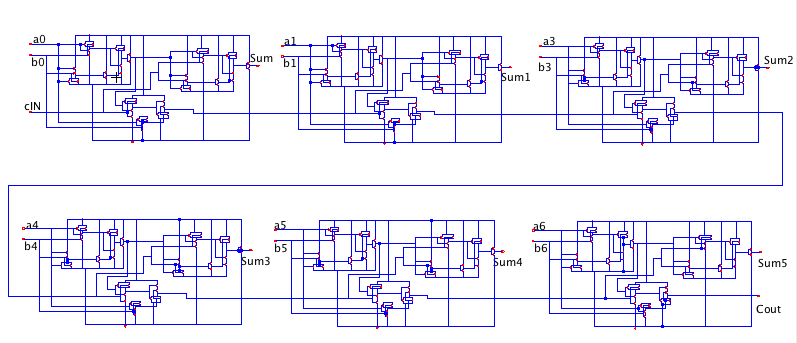
In the image below we show one section zoomed in of the 6 bit adder. It is 1bit portion of the entire schematic. In it you can see the inputs A0 B0 Sum and Cin. Each other adder has the same layout with its corresponding inputs i.e. A1 A3 B2 B3 etc. In this schematic we assume that specific calculations will be introduced such as 1+4=5. For the parameters we believe the calculations can go up to 2^6. The length is 1.2u and the width would be 0.6u for NMOS and length is 0.6u and width is 2.4u for the PMOS.

**Figure1: Schematic of 1bit full adder with carry in(Part of 6 bit adder)**





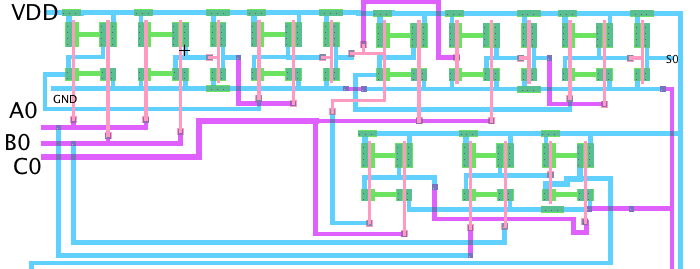
**Figure 2: Schematic of 6 bit full adder (Obtained by Cascading 6 1-bit adders)**



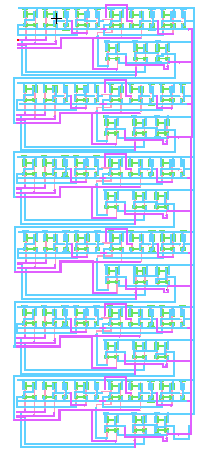
In the above schematic if we zoom out you can see the entire schematic with all six adders. We can see how all the carry ins are connected and lead out into a carry out function and the bottom right.

In the picture below we see a zoomed in version of the layout completed using electric. If we look closely we see the inputs A0 B0 and Cin that continues down to the lower LCU system. This picture shows one completed adder and you can see the metals connecting down to the other inputs and also the other carrys.

**Figure 3: Layout of 1bit adder**



**Figure 4: Layout of 6 bit full adder (Obtained by Cascading 6 1-bit adders)**

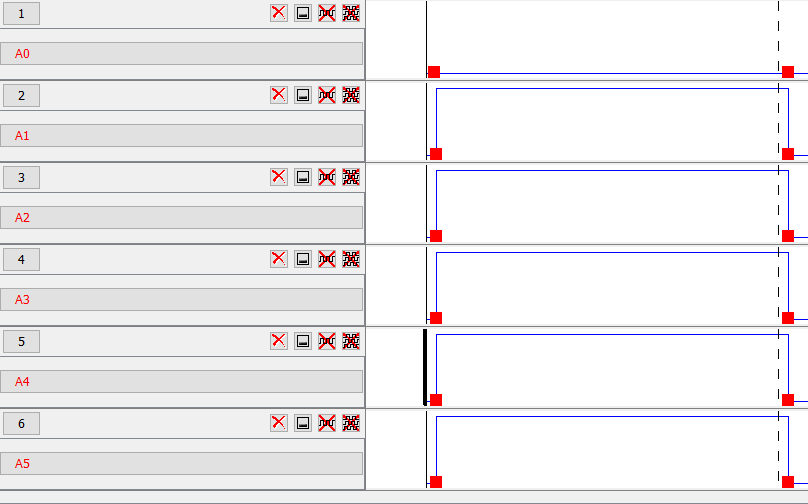


In the photo above we show entire layout. Due to its size we cant every single label but as explained before it is 6 repeated adders shown above, difference is that where the above Cin is located the last adder in the layout has a Cout.

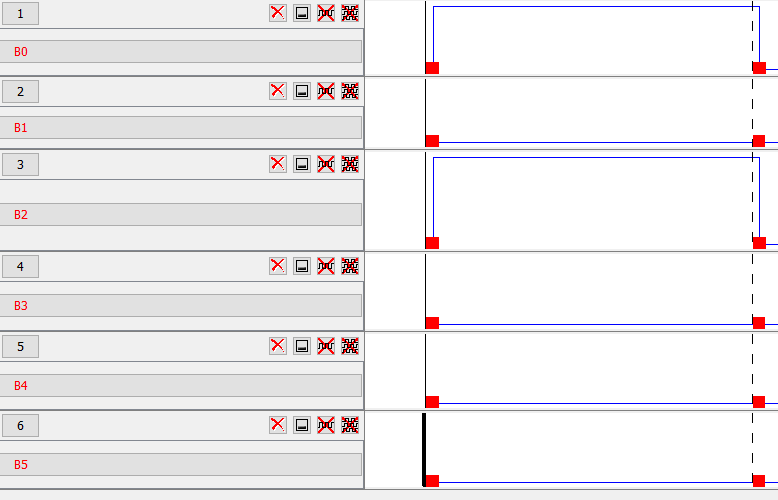
**IRSIM Simulation:**

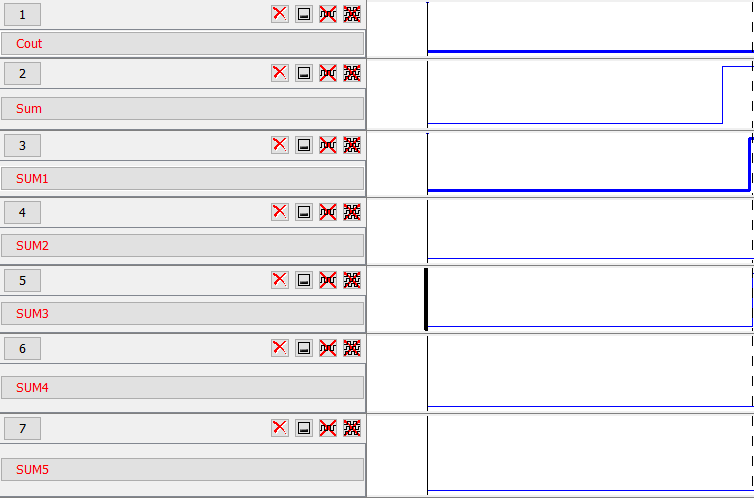
Below we have the IRSIM for the addition of -2 + 5 = 3 which is basically 5 – 2 = 3. Based the on the simulation below we can see that our adder is working correctly. Using the inputs (A0 = 0, A1=1,A2=1 , A3=1, A4=1,A5=1) + (CIN =0) (B0=1, B1=0, B2=1, B3=0, B4=0, B5=0) AND SUM (SUM=1, SUM1=1,SUM2=0, SUM3=0, SUM4=0, SUM5 =0) COUT = 0 we get the total for sum being 3.

**Figure 5: IRSIM of -2 + 5 = 3**

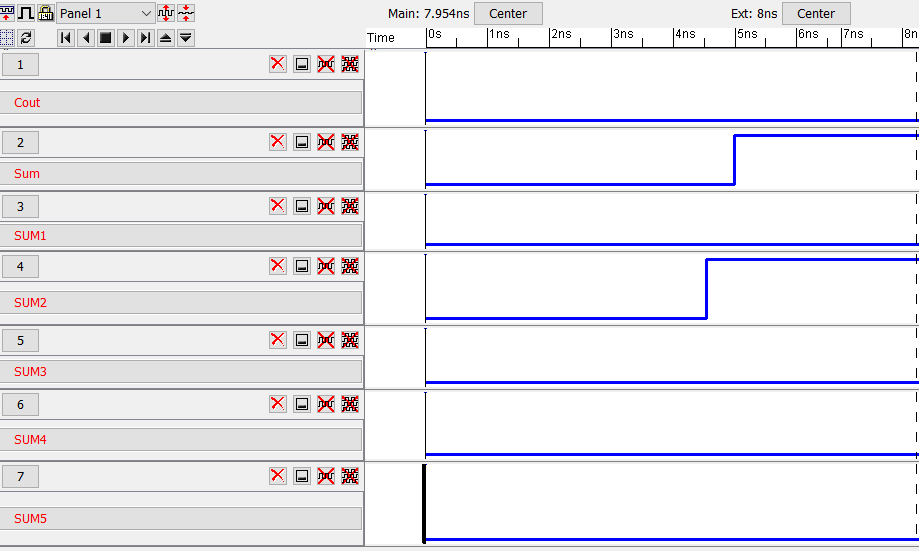
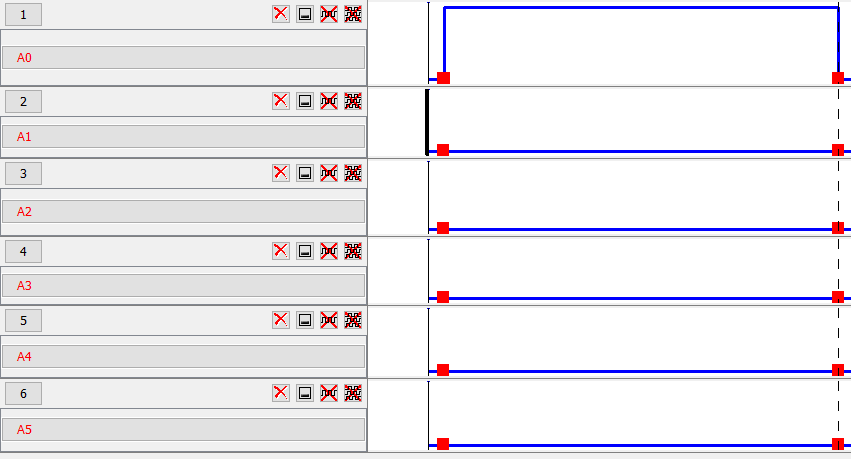




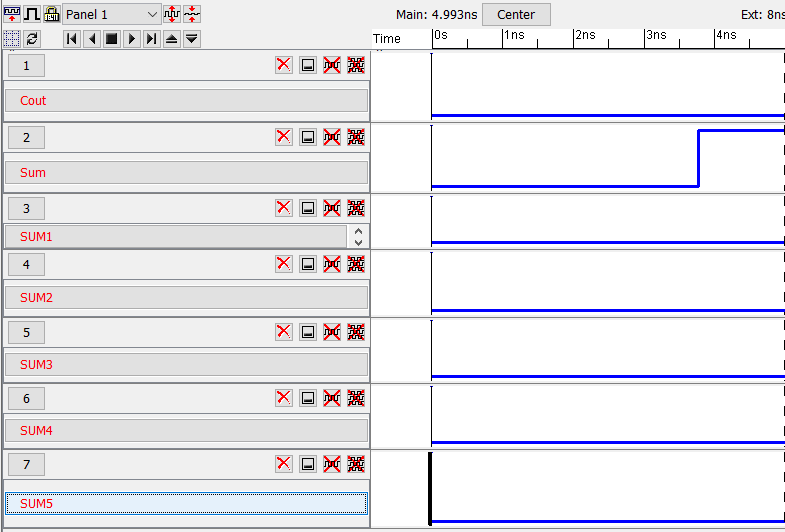
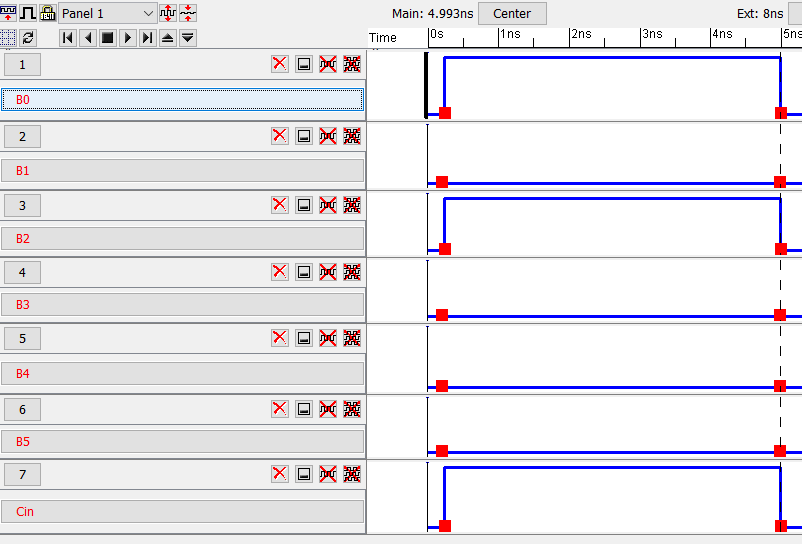
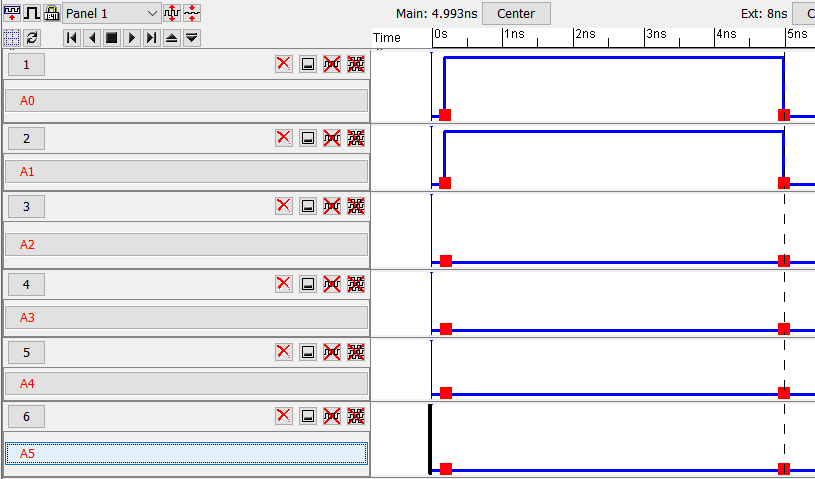




Next we work on 1+4 = 5 and if you look at the simulations below you can clearly see that using the inputs (A0 = 1, A1=0,A2=0 , A3=0, A4=0,A5=0) + (CIN =0) (B0=0, B1=0, B2=1, B3=0, B4=0, B5=0) AND SUM (SUM=1, SUM1=0,SUM2=1, SUM3=0, SUM4=0, SUM5 =0) COUT = 0 we get our expected answer of 5. So far everything is working properly and as expected.

**Figure 6: IRSIM of 1 + 4 = 5**

Finally we do our final calculation of 3 + -5 = -2 by using inputs of (A0 = 1, A2=1 , A3=0, A4=0,A5=0) -(CIN =1) (TO MAKE SUBTRACTION) (B0=1, B1=0, B2=1, B3=0, B4=0, B5=0). As you can see for the solution we get 000001 and Cout as 0, but when you take the 2's complement you get the correct answer which is 111110 = -2. Thus showing that our project works correctly. We can see that our 6bit adder passes all the verifications that we implemented them through and correctly computes addition and subtraction.

**Figure 7: IRSIM of 3 + -5 = -2**

**LTSPICE Verifications:**

Below is the LTSPICE code used for our project.

**LT spice code and N and P mos transistor measurements:**

\*\*\* SPICE deck for cell 6bit-full-adder{sch} from library Full-adder

\*\*\* Created on Mon Nov 23, 2015 16:01:37

\*\*\* Last revised on Tue Nov 24, 2015 21:26:58

\*\*\* Written on Tue Nov 24, 2015 21:27:26 by Electric VLSI Design System,

\*\*\* version 9.05

\*\*\* Layout tech: mocmos, foundry MOSIS

\*\*\* UC SPICE \*\*\* , MIN\_RESIST 4.0, MIN\_CAPAC 0.1FF

.globalgndvdd

\* Spice Code nodes in cell cell '6bit-full-adder{sch}'

VDD VDD 0 DC 3.3

VGND GND 0 DC 0

VIN1 A0 0 PULSE(3.3 0 0 100p 100p 20n 40n)

VIN2 A1 0 DC 0

VIN3 A2 0 DC 0

VIN4 A3 0 DC 0

VIN5 A4 0 DC 0

VIN6 A5 0 DC 0

VIN7 B0 0 DC 0

VIN8 B1 0 DC 0

VIN9 B2 0 PULSE(3.3 0 0 100p 100p 20n 40n)

VIN10 B3 0 DC 0

VIN11 B4 0 DC 0

VIN12 B5 0 DC 0

VIN13 Cin 0 DC 0

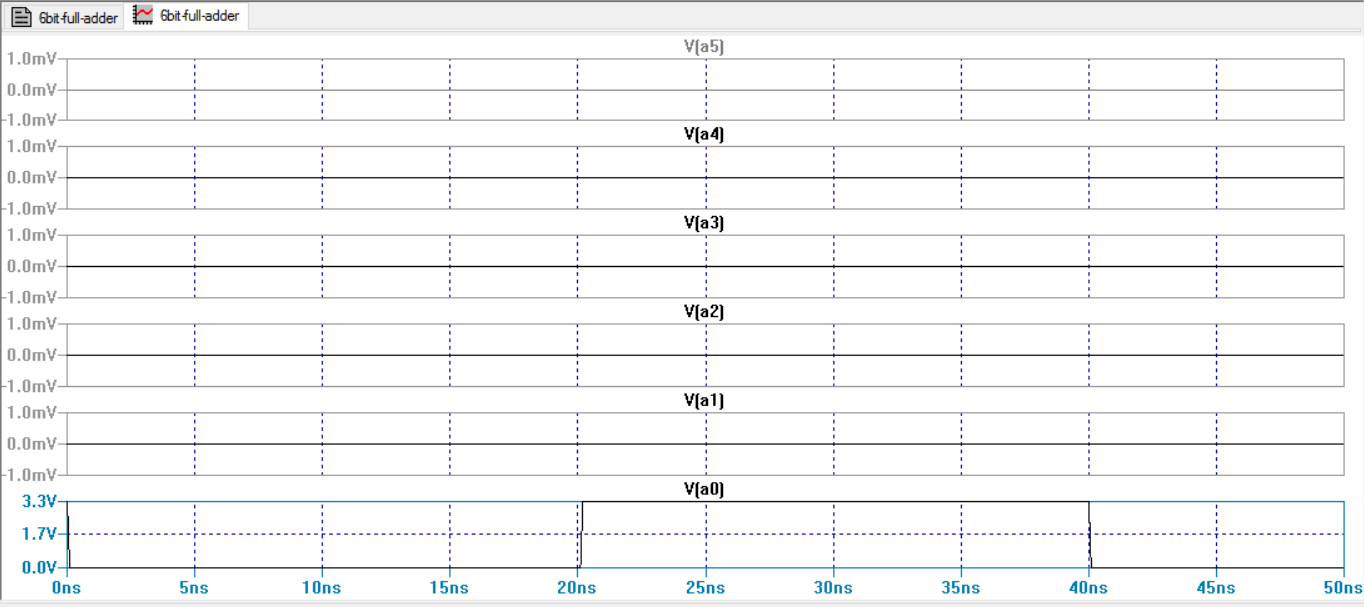
.TRAN 0 50n

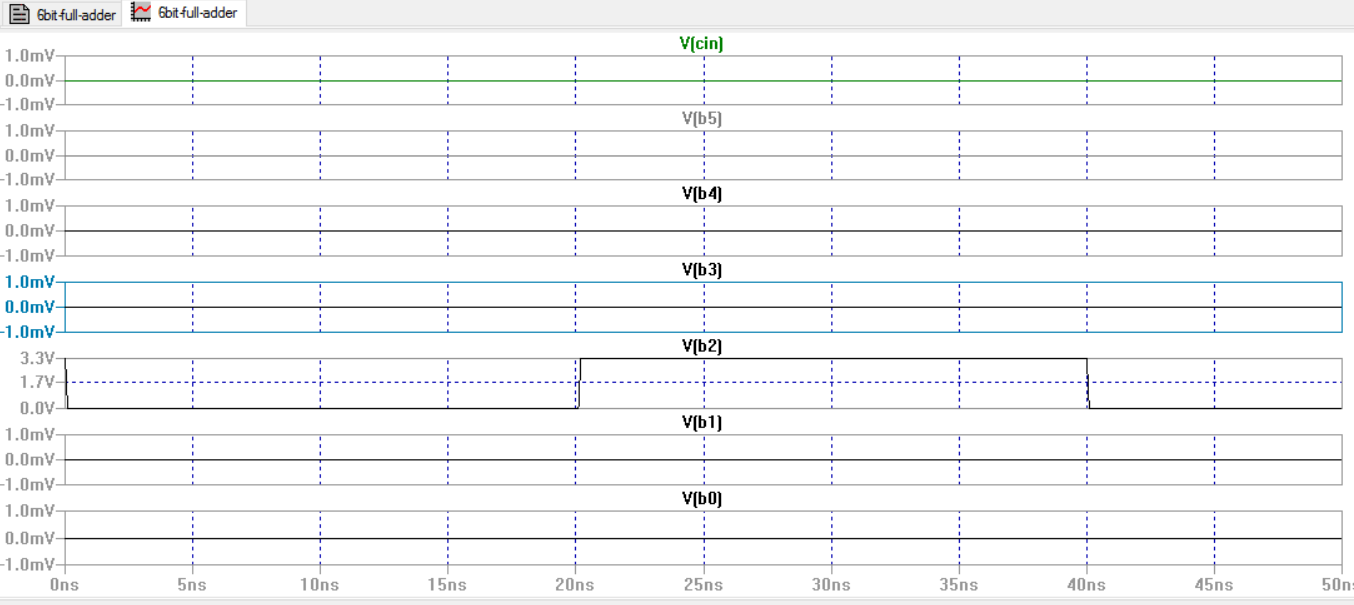
.include C:\Users\Vivek\Documents\MODEL\_MOS.txt

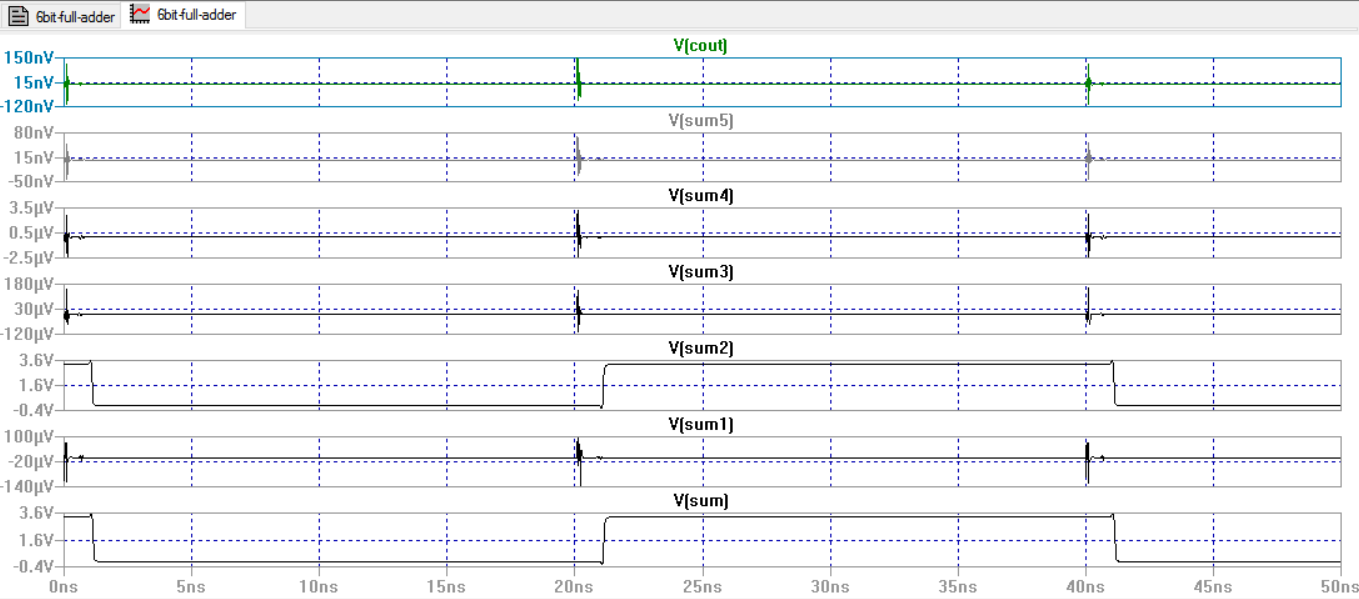
.END

Below is the simulation for 1+4 = 5 using LTSPICE, the delay in input vs. output pulses = 21.59ns - 20.28ns = 1.31nanoseconds. This is the measured delay for our look ahead carry adder.

**Figure 8: LTSpice simulation of** 1 + 4 = 5







The above LTSPICE simulation matches our IRSIM simulation that shows 1+4=5. As we can see there is a delay for the calculation as calculated above. But the sum is still exactly what was expected.

**Conclusions:**

In conclusion we saw that the adder worked as expected. We noticed that putting in the different inputs for addition and subtraction calculated the correct answer just as we expected. We noticed the calculated delay was pretty low and was very good compared to a ripple carry adder. The simulations we used also showed us that our theory was indeed completed. Our Layout using electric showed us that we designed everything properly and we chose a correct Euler's path.

**References:**

Thomas K. Callaway and Earl E. Swartzlander, “Estimating the Power consumption of CMOS Adders,” Dept. of Elect.Engr. and Comp.Engr.*,*Unv. Of Texas, Austin,1993.